REMARKS

A Notice of Allowance was mailed for this Application on June 11, 2009. In the Notice of Allowance, the Examiner indicated that Claims 1-19 were allowed. Also, claims 8, 9 and 12 were amended in the Notice of Allowance by Examiner's Amendment.

Independent claims 1, 5, 8 and 14 are current being amended, and new dependent claims 20-26 are being added, leaving claims 1-26 for the Examiner's consideration. Applicants believe support for the claim amendments and new claims is provided explicitly and/or inherently in the application as originally filed, and thus, that no new matter has been added. The amendments to the independent claims are not narrowing. Applicants believe that the independent claims as amended are still patentable over the cited references for at least some of the reasons provided in the Reply filed on February 27, 2009, as explained below.

This Amendment is filed together with a Request for Continued Examination (RCE) and the required fees.

Applicants respectfully request examination of the claims as amended, and that another Notice of Allowance be issued.

1. Independent Claim 1

Independent claim 1, as amended, still requires, inter alia, that

each of a plurality of channels includes

> "a buffer management unit ... configured to control a rate at which samples are read from the input buffer to achieve a target difference between the values of the read and write pointers;
>
> wherein for a first one of the channels, the target difference comprises a predetermined value; and
>
> wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels."

Applicants respectfully assert that the cited references, alone or in combination, do not teach or suggest the above features, as explained below.

Cory discusses both a master elastic buffer and slave elastic buffers. For this discussion, Applicants again assume that the Examiner is asserting that Cory's master elastic buffer is part of a master channel that is analogous to the claimed "first one of the channels"; and that Cory's slave elastic buffers are part of slave channels that are analogous to the claimed "the remainder of the channels".

1.a Cory does not teach or suggest that each of a plurality of channels includes "a buffer management unit ... configured to control a rate at which samples are read from the input buffer to achieve a target difference between the values of the read and write pointers; wherein for a first one of the channels, the target difference comprises a predetermined value" as required by claim 1

It was asserted in the Office Action of October 30, 2008, that column 19, lines 7-23 of Cory teaches that Cory's controls a read pointer to achieve a target difference for a first one of the channels. Applicants respectfully disagree, as explained in the Reply filed on February 27, 2009, and reiterated below. For the convenience of the Examiner, column 18, line 61 – column 19 line 31 (which includes Column 19, lines 7-23) of Cory is quoted verbatim below (with emphasis added).

> "Operational control circuit 211 also ensures that clock correction operations are handled properly by read control circuit 213. As input data stream Din is written to memory space 220, operational control circuit 211 monitors input data stream Din and write address Waddr to keep track of the locations of correction sequences (and also channel alignment blocks) within memory space 220. **Operational control circuit 211 evaluates the "fullness" of memory space 220 (as indicated by the difference between the read and write addresses), and it determines whether to do an accelerating or delaying clock correction, or continue reading normally when read address Raddr_a or read address Raddr_b reaches a correction sequence.**
>
> To execute these various actions, operational control circuit 211 provides a plurality of control signals to read control circuit 213. To initiate clock correction operations, operational control circuit 211 can generate clock correction signals CC_enb and CC_enb2, and to specify the appropriate clock correction increments, operational control circuit 211 can generate address/increment signals incr_addr and incr_addr2. Note that address/increment signals incr_addr and incr_addr2 can specify either an increment (positive or negative) by which the current address is modified, or an absolute address that replaces the current address. Operational control circuit 211 can also provide an optional stagger control signal STAG to control clock correction operations taking place across multiple read clock cycles. Finally, operational control circuit 211 can provide a channel bonding signal CB_load to control channel bonding operations, to be discussed in a subsequent section. Note that clock correction signal CC_enb2, address/increment signal incr_addr2 and stagger control signal STAG are shown as optional (using dotted lines) and can therefore represent any number of additional control signals required to perform the clock correction operations described previously. Note

further that circuit 211 can maintain internal copies of write address Waddr and read address Raddr_b to ensure generation of the elastic buffer control signals in a timely fashion."

In the first paragraph quoted above (i.e., Column 18, line 61 – Column 19, line 6), Cory explains that its operational control circuit can evaluate the fullness of its memory space based on the difference between the read and write addresses. However, this portion of Cory never states that it controls a rate at which samples are read from an input buffer to achieve a target difference between the values of the read and write pointers/addresses for one of the channels (e.g., Cory's master channel), where **the target difference comprises a predetermined value**, as is required by claim 1. In other words, while Cory determines a difference between read and write addresses, Cory does so to determine the fullness of the memory, **NOT** to control a rate at which samples are read from the buffer of Cory's master channel to achieve a target difference in the master channel that is a predetermined value.

Further, in the first paragraph quoted above, Cory states that it determines whether to perform an accelerating or delaying clock correction, or continue reading normally "when read address Raddr_a or read address Raddr_b reaches a **correction sequence**". As defined in Cory at Column 2, lines 21-23, a "correction sequence" is defined as the smallest set of data blocks that may be omitted or added for clock correction operations.

In the second paragraph quoted above (i.e., Column 19, lines 7 – 31), Cory explains that address/increment signals (incr_addr and incr_addr2) can specify either an increment (positive or negative) by which a current address is modified, or an absolute address that replaces the current address. However, this portion of Cory never states that the current address is modified or replaced in order to achieve a target difference between the values of the read and write pointers/addresses for one of the channels (e.g., Cory's master channel), where **the target difference comprises a predetermined value**, as is required by claim 1.

Further, none of the other applied references appear to teach or suggest this deficiency of Cory.

1.b Cory does not teach or suggest "wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels" as required by claim 1

Claim 1 further specifies "wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels". Thus if the predetermined value of the target difference is, e.g., 100, but the actual difference between the read and write pointers of the first one of the channels is 105, then for the other channels (i.e., the remainder of the channels) the buffer management unit is configured to control the rate at which samples are read from the input buffer (of those remaining channels) to achieve a difference of 105, to attempt to synchronize the remainder of the channels with the first one of the channels. This is useful because it is better to have the phase of a plurality of channels similarly offset from a desired phase than to have all the channels close to the desired phase but offset from each other. In other words, in the embodiment of claim 1, the remainder of the channels (e.g., the slave channels) will track the offset of the first one of the channels (e.g., the master channel) in order to match the phase delay through all of the channels of the system, which is useful because for an audio system time alignment is important. Thus, this approach maintains alignment even if a time base of the first one of the channels (e.g., the master channel) is drifting.

It was asserted in the Office Action of October 30, 2008 that Cory teaches "wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels" at Column 29, lines 56-66. Applicants respectfully disagree, as explained in the Reply filed on February 27, 2009, and reiterated below. For the convenience of the Examiner, Column 29, lines 56-66 of Cory is quoted verbatim below.

> "Note that after completion of a channel bonding operation, the resulting data alignment could be destroyed if all the elastic buffers executed different clock corrections (type and/or timing). Therefore, according to an embodiment of the invention, master elastic buffer 200(1) can maintain data alignment produced by controlling clock correction operations for all slave elastic buffers as well as for itself. Controller 210(1) in master elastic buffer 200(1) could control channel alignment and clock correction by means of the CC_enb, CB_load, STAG, and incr_addr signal connections as shown in FIG. 2d. According to an embodiment of the invention, these signals could be asserted

early and buffered inside controllers 210(1) and 210(2) for subsequent assertion at an appropriate time, thereby accommodating signal routing delays between elastic buffers."

The above quoted portion of Cory explains that the master elastic buffer can maintain data alignment for all the slave elastic buffers and itself by means of the CC_enb, CB_load, STAG, and incr_addr signal. CC_enb is a clock correction signal, CB_load is a channel bonding signal, STAG is stagger control signal, and incr_addr is an address increment signal. Thus, the above quoted section of Cory merely explains that the master elastic buffer can control itself and the slave buffers by controlling clocks, by channel bonding, by staggering and/or by incrementing addresses. However, this portion of Cory, and other portions of Cory, do not teach or suggest that the rate at which samples are read from the input buffers of the remainder of the channels (presumably the slave channels) is controlled specifically to achieve the actual difference between the values of the read and write pointers of the first one of the channels (presumably the master channel).

Further, none of the other applied references appear to teach or suggest this deficiency of Cory.

2. Independent Claim 5

Independent claim 5, as amended, still requires, inter alia, that

each of a plurality of channels includes

"a sample rate converter configured to receive samples of an input audio data stream, store the samples in an input buffer, retrieve samples from the input buffer, and convert the samples to a re-sampled audio data stream, and

a buffer management unit coupled to the input buffer and configured to maintain a write pointer indicating a position in the input buffer to which a next sample will be written and a read pointer indicating a position in the input buffer from which a next sample will be read, wherein the buffer management unit is configured to determine an actual difference between the values of the read and write pointers, wherein the buffer management unit is further configured to

control a rate at which samples are read from the input buffer to achieve a target difference between the values of the read and write pointers;

wherein for a first one of the channels, the target difference comprises a predetermined value;

wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels".

For similar reasons to those discussed above with reference to independent claim 1, Applicants assert the applied references to not teach or suggest these features of independent claim 5.

Further, claim 5 as amended also requires the following features which are not believed to be taught or suggested by the applied references:

"wherein for each channel the sample rate converter further comprises a phase selection unit coupled to the buffer management unit, wherein a phase output signal of the phase selection unit is transmitted to the buffer management unit and wherein the phase output signal controls reads from the input buffer;

wherein for each channel the sample rate converter further comprises a rate estimator counter, wherein the rate estimator counter is configured to provide a sample rate count to a low pass filter, wherein the low pass filter is configured to filter the sample rate count and to provide the filtered sample rate count to the phase selection unit, and wherein the phase selection unit is configured to generate the phase output signal based upon the filtered sample rate count; and

wherein for each channel the buffer management unit is configured to transmit an error signal to the low pass filter and wherein the low pass filter is configured to use the error signal as an offset to the sample rate count."

For at least the above reasons, Applicants respectfully assert that claim 5 as amended is still patentable over the applied references.

3. Independent Claim 8

Independent claim 8, as amended, still requires, inter alia, that

"determining a difference between values of a read pointer and a write pointer in each of a plurality of buffers;

controlling a first rate at which samples are read from a first one of the buffers to drive the difference between the corresponding read and write pointers to a predetermined value; and

controlling rates at which samples are read from each of the remaining buffers to drive the difference between the corresponding read and write pointers to the difference between the read and write pointers of the first buffer."

For similar reasons to those discussed above with regards to claim 1, Applicants assert that independent claim 8 as amended is still patentable over the applied references.

4. Independent Claim 14

Independent claim 14, as amended, still requires, inter alia, that

"a plurality of buffers, including a master buffer and one or more slave buffers;

wherein each buffer has a corresponding

write pointer indicating a position in the buffer to which a next received value will be written,

read pointer indicating a position in the buffer from which a next output value will be read, and

controller configured to determine an actual differential between the read and write pointers and to control a corresponding rate at which samples are read from the buffer to achieve a target differential between the read and write pointers;

wherein for the master buffer, the target differential comprises a predetermined value; and

wherein for the slave buffers, the target differential comprises the actual differential between the read and write pointers of the buffer."

For similar reasons to those discussed above with regards to claim 1, Applicants assert that independent claim 14 as amended is still patentable over the applied references.

5. Conclusion

For at least the reasons specified above, Applicants respectfully assert that the claims as amended are still patentable, and another Notice of Allowance is respectfully requested.

The Examiner is respectfully requested to telephone the undersigned if he can assist in any way in expediting issuance of a patent.

The Commissioner is authorized to charge the required fees and any underpayment of fees or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this reply, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: September 4, 2009

By: /Jeffrey R. Kurin/
Jeffrey R. Kurin
Reg. No. 41,132

FLIESLER MEYER LLP
650 California Street, 14th Floor
San Francisco, CA 94108
Telephone: (415) 362-3800
Facsimile: (415) 362-2928
Customer No. 23910